WHAT IS CLAIMED IS:

1. A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$, said demodulator comprising:

a Logic 0 input detector capable of comparing each of said M binary bits of said serially received orthogonal modulation codes to a Logic 0 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur;

a summation circuit comprising S accumulators;

a Logic 0 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 0 switch array is capable of coupling an output of said Logic 0 input detector to a first input of a Kth one of said S accumulators;

a storage array capable of storing said S orthogonal modulation codes; and

control circuitry capable of synchronously applying the M bits in a Kth one of said S orthogonal modulation codes in said storage array as a switch control signal to said Kth switch in said Logic 0 switch array so that each Logic 0 binary data in said Kth orthogonal modulation code closes said Kth switch in said Logic 0

switch array, thereby connecting the output signal of said Logic 0 input detector to said first input of said Kth accumulator.

2. The demodulator as set forth in Claim 1 further comprising:

a Logic 1 input detector capable of comparing each of said M binary bits of said serially received orthogonal modulation codes to a Logic 1 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur; and

a Logic 1 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 1 switch array couples an output of said Logic 1 input detector to a second input of said Kth accumulator;

wherein said control circuitry is capable of synchronously applying the M bits in said Kth orthogonal modulation code in said storage array as a switch control signal to said Kth switch in said Logic 1 switch array so that each Logic 1 binary data in said Kth orthogonal modulation code closes said Kth switch in said Logic 1 switch array, thereby connecting the output signal of said Logic 1 input detector to said second input of said Kth accumulator.

3. The demodulator as set forth in Claim 2 wherein each Logic 1 binary data in said Kth orthogonal modulation code opens said Kth switch in said Logic 0 switch array, thereby disconnecting the output signal of said Logic 0 input detector from said first input of said Kth accumulator.

4. The demodulator as set forth in Claim 3 wherein each Logic 0 binary data in said Kth orthogonal modulation code opens said Kth switch in said Logic 1 switch array, thereby disconnecting the output signal of said Logic 1 input detector from said second input of said Kth accumulator.

5. The demodulator as set forth in Claim 2 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

6. The demodulator as set forth in Claim 5 wherein said code selection circuit outputs one of 2^N N-bit data symbols corresponding to said identified accumulator contain said maximum value.

7. The demodulator as set forth in Claim 6 wherein N = 6 and $M = 2^N = 64$.

8. The demodulator as set forth in Claim 7 wherein S = 64.

9. The demodulator as set forth in Claim 8 wherein said orthogonal modulation codes are Walsh codes.

10. A code division multiple access (CDMA) wireless network comprising a plurality of base transceiver stations capable of communicating with access terminals located in a coverage area of said wireless network, wherein a first one of said plurality of base transceiver stations comprises:

a demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$, said demodulator comprising:

a Logic 0 input detector capable of comparing each of said M binary bits of said serially received orthogonal modulation codes to a Logic 0 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur;

a summation circuit comprising S accumulators;

a Logic 0 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 0 switch array is capable of coupling an output of said Logic 0 input detector to a first input of a Kth one of said S accumulators;

a storage array capable of storing said S orthogonal modulation codes; and

control circuitry capable of synchronously applying the M bits in a Kth one of said S orthogonal modulation codes in said storage array as a switch control signal to said Kth switch in said Logic 0 switch array so that each Logic 0 binary data in said Kth orthogonal modulation code closes said Kth switch in said Logic 0 switch array, thereby connecting the output signal of said Logic 0 input detector to said first input of said Kth accumulator.

11. The CDMA wireless network as set forth in Claim 10 further comprising:

a Logic 1 input detector capable of comparing each of said M binary bits of said serially received orthogonal modulation codes to a Logic 1 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur; and

a Logic 1 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 1 switch array couples an output of said Logic 1 input detector to a second input of said Kth accumulator;

wherein said control circuitry is capable of synchronously applying the M bits in said Kth orthogonal modulation code in said storage array as a switch control signal to said Kth switch in said Logic 1 switch array so that each Logic 1 binary data in said Kth orthogonal modulation code closes said Kth switch in said Logic 1 switch array, thereby connecting the output signal of said Logic 1 input detector to said second input of said Kth accumulator.

12. The CDMA wireless network as set forth in Claim 11 wherein each Logic 1 binary data in said Kth orthogonal modulation code opens said Kth switch in said Logic 0 switch array, thereby disconnecting the output signal of said Logic 0 input detector from said first input of said Kth accumulator.

13. The CDMA wireless network as set forth in Claim 12 wherein each Logic 0 binary data in said Kth orthogonal modulation code opens said Kth switch in said Logic 1 switch array, thereby disconnecting the output signal of said Logic 1 input detector from said second input of said Kth accumulator.

14. The CDMA wireless network as set forth in Claim 11 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

15. The CDMA wireless network as set forth in Claim 14 wherein said code selection circuit outputs one of 2^N N-bit data symbols corresponding to said identified accumulator contain said maximum value.

16. The CDMA wireless network as set forth in Claim 15 wherein N = 6 and $M = 2^N = 64$.

17. The CDMA wireless network as set forth in Claim 16 wherein S = 64.

18. The CDMA wireless network as set forth in Claim 17 wherein said orthogonal modulation codes are Walsh codes.

19. For use in a base station of a wireless network capable of communicating with mobile stations located in a coverage area of the wireless network, a method of demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of the orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$, the method comprising the steps of:

in a Logic 0 input detector, comparing each of the M binary bits of the serially received orthogonal modulation codes to a Logic 0 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur;

retrieving from a storage array the Kth one of S orthogonal modulation codes stored therein;

synchronously applying the M bits of the Kth orthogonal modulation code as a switch control signal to a Kth switch in a Logic 0 switch array comprising S switches, wherein the Kth switch in the Logic 0 switch array is capable of coupling an output of the Logic 0 input detector to a first input of a Kth one of S accumulators, and wherein each Logic 0 binary data in the Kth orthogonal modulation code closes the Kth switch in the Logic 0 switch array, thereby connecting the output signal of the Logic 0 input detector to the first input of the Kth accumulator.

20. The method as set forth in Claim 19 further comprising the steps of:

in a Logic 1 input detector, comparing each of the M binary bits of the serially received orthogonal modulation codes to a Logic 1 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur;

synchronously applying the M bits of the Kth orthogonal modulation code as a switch control signal to a Kth switch in a Logic 1 switch array comprising S switches, wherein the Kth switch in the Logic 1 switch array is capable of coupling an output of the Logic 1 input detector to a second input of the Kth accumulator, and wherein each Logic 1 binary data in the Kth orthogonal modulation code closes the Kth switch in the Logic 1 switch array, thereby connecting the output signal of the Logic 1 input detector to the second input of the Kth accumulator.